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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,989	06/20/2003	John P. Banning	TRAN-P055	7126

7590 06/02/2006

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EXAMINER	
LAI, VINCENT	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,989	BANNING ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --.

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisor FRITZ FLEMING PRIMARY EXAMINER GROUP 2100 5/26/2006 AU 2181

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Acknowledgment is made of the amendment of the specification and title filed by applicant on 20 March 2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 11-15, and 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Yates, Jr. et al (U.S. Patent # 6,397,379 B1).

As per claim 1, Yates, Jr. et al discloses method of recovering a pointer to a non-native instruction, said method comprising:

executing a commit operation (Column 44, lines 42-43: There is a transfer of control to another instruction, which indicates commitment);

accessing a translation of a code sequence non-native instructions to a code sequence of native instructions (Column 18, lines 61-63: Translation is done in changing states of the processor);

registering a first address for a native instruction associated with said commit operation (Column 44, lines 23-37: Action is part of the context switching as described); and

registering a second address used for recovering a non-native instruction associated with said commit operation (Column 44, lines 23-37: Action is part of the context switching as described).

As per claim 2, Yates, Jr. et al discloses wherein said first address and said second address each comprise a program counter value for said native instruction, wherein said native instruction comprises a pointer to the effective instruction pointer value for said non-native instruction (Column 44, lines 23-29: links must be made in order to context switch, and return to the original process).

As per claim 3, Yates, Jr. et al discloses wherein said executing and accessing further comprise:

executing a first commit operation (Column 44, lines 42-43);

accessing a first translation of non-native instructions to a first code sequence of native instructions (Column 18, lines 61-63), said first code sequence comprising a first native instruction associated with said first commit operation (Column 44, lines 42-43);

executing a second commit operation (Column 44, lines 45-47: the first commit induces a change, which acts as a second commit); and

accessing a second translation of non-native instructions to a second code sequence of native instructions (Column 18, lines 61-63), said second code sequence comprising a second native instruction associated with said second commit operation (Column 44, lines 42-43).

As per claim 11, Yates, Jr. et al discloses wherein said native instruction comprises a first bit, a second bit, a third bit, and a plurality of pointer bits, said first bit for causing said commit operation to be executed and a program counter value corresponding to said native instruction to be registered (Column 44, lines 50-54), said second bit for indicating whether said program counter value is to be registered (Column 43, lines 22-24), and depending on the value of said third bit, said pointer bits instruction pointer for said non-native instruction or to another instruction that pointing to the effective can be used for recovering said effective instruction pointer (Column 43, lines 22-24).

As per claim 12, Yates, Jr. et al discloses using information in said plurality of

pointer bits to identify a mode of operation associated with said translating (Column 1, lines 44-50).

As per claim 13, Yates, Jr. et al discloses using said second address to identify a translation comprising said code sequence of native instructions (Column 44, lines 23-29).

As per claim 14, Yates, Jr. et al discloses a method of recovering a non-native instruction during execution of native instructions, said method comprising:

accessing a translation of a code sequence of non-native instructions to a code sequence of native instructions, said code sequence of native instructions advancing from a commit point (Column 18, lines 61-63);

performing a rollback operation to return to said commit point using a first address to locate a native instruction associated with said commit point (Column 44, lines 23-29); and

in conjunction with said rollback operation, using a second address to recover a non-native instruction associated with said commit point (Column 44, lines 23-29).

As per claim 15, Yates, Jr. et al discloses wherein said code sequence of native instructions comprises a first code sequence of native instructions and a second code sequence of native instructions, said first code sequence demarcated by a first commit

operation and comprising a first native instruction associated with said first commit operation, and said second code sequence demarcated by a second commit operation and comprising a second native instruction associated with said second commit operation (Column 44, lines 23-29).

As per claim 23, Yates, Jr. et al discloses a method of recovering a non-native instruction during execution of native instructions, said method comprising:

accessing a translation of a code sequence of non-native instructions to a code sequence of native instructions, said translation demarcated by a commit point (Column 18, lines 61-63);

taking an exception identified during execution of said translation (Column 18, lines 38-63);

reading an address in a register, said address pointing to a native instruction having an indicator bit and a plurality of pointer bits, wherein depending on the value of an effective instruction pointer for a non-native instruction associated with said commit point or to information that can be used for recovering said effective instruction pointer (Column 44, lines 23-37).

As per claim 24, Yates, Jr. et al wherein said information comprises another instruction that points to said effective instruction pointer (Column 44, lines 23-29).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4-6, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yates, Jr. et al (U.S. Patent # 6,397,379 B1) in view of Spix et al (U.S. Patent # 6,195,676 B1).

As per claim 4, Yates, Jr. et al teaches the execution a commit operation with respect to a code sequence of native instructions (Column 44, lines 42-43).

Yates, Jr. et al does not teach wherein said second code sequence of native instructions is executed in a loop, said first code sequence of native instructions establishing conditions for said loop, wherein said second commit operation is executed each time said loop is executed.

Spix et al teaches the vectorization of loops in order to be able to split up loops as to allow for context switch switches in the middle of loops (Column 44, lines 56-62).

Therefore it would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Yates, Jr. et al to include the use of loops.

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Yates, Jr. et al by the teachings of Spix et

al, because it would allow the breaking up of loops and thus avoiding delays in committing a context switch.

As per claim 5, Yates, Jr. et al discloses wherein said first address and said second address each comprise a program counter value for said second native instruction (Column 44, lines 23-29: Part of a context switch operation).

As per claim 6, Yates, Jr. et al discloses wherein said second native instruction comprises a pointer to said first native instruction, said first native instruction comprising a pointer to the effective instruction pointer value for said non-native instruction (Column 44, lines 23-29: Needed for switching back and is done as part of a context switch).

As per claim 16, Yates, Jr. et al in light of Spix et al discloses wherein said second code sequence of native instructions is executed in a loop, said first code sequence of native instructions establishing conditions for said loop, wherein said second commit operation is executed each time said loop is executed (As explained in rejection of claim 4).

As per claim 17, Yates, Jr. et al discloses wherein said first address and said second address each comprise a program counter value for said second native instruction (Column 44, lines 23-29).

As per claim 18, Yates, Jr. et al in light of Spix et al discloses wherein said rollback operation is prompted by an event that is external to said loop, said event potentially causing a change to said conditions (Column 44, lines 23-29: Reference does not involve a loop for operation).

As per claim 19, Yates, Jr. et al discloses wherein said event is a direct memory access operation (Column 15, lines 53-60).

4. Claims 8-10, 25, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yates, Jr. et al (U.S. Patent # 6,397,379 B1) in view of Chung et al (U.S. Patent # 6,044,475).

As per claim 8, Yates, Jr. et al teaches the use of code sequence of native instruction calls (Column 44, lines 42-43).

Yates, Jr. et al does not teach wherein said first code sequence of native instructions calls said second code sequence of native instructions as a subroutine.

Chung et al teaches the use of subroutines in running checkpoints to allow for easier splitting of instruction when a context switch occurs (Column 9, lines 47-54).

Therefore it would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Yates, Jr. et al to include the use of subroutines.

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Yates, Jr. et al by the teachings of Chung et al, because the use of subroutines allow for easier context switch/state saving.

As per claim 9, Chung et al discloses wherein said subroutine is callable by code sequences other than said first code sequence (Column 8, lines 65- column 9, lines 2: Any code can all the subroutine, which is often done automatically).

As per claim 10, Yates, Jr. et al discloses wherein said first address comprises a program counter value for said second native instruction and said second address comprises a program counter for said first native instruction, wherein said first native instruction comprises a pointer to the effective instruction pointer for said non-native instruction (Column 44, lines 23-29).

As per claim 25, Chung et al discloses wherein said information comprises a subroutine that provides said effective instruction pointer (Column 9, lines 47-54).

As per claim 29, Yates, Jr. et al discloses wherein said translation comprises a first code sequence of native instructions that calls a second code sequence of native instructions as a subroutine, wherein said address points to an instruction within said first code sequence that has pointer bits that point to said effective instruction pointer (Column 44, lines 23-29).

5. Claims 7, 20-22, and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yates, Jr. et al (U.S. Patent # 6,397,379 B1) in view of Spix et al (U.S. Patent # 6,195,676 B1) and Chung et al (U.S. Patent # 6,044,475).

Yates, Jr. et al teaches the execution a commit operation with respect to a code sequence of native instructions (Column 44, lines 42-43).

Yates, Jr. et al does not teach wherein code sequence of native instructions is executed in a loop and calls another code sequence of native instructions as a subroutine.

Spix et al teaches the vectorization of loops in order to be able to split up loops as to allow for context switch switches in the middle of loops (Column 44, lines 56-62).

Chung et al teaches the use of subroutines in running checkpoints to allow for easier splitting of instruction when a context switch occurs (Column 9, lines 47-54).

Therefore it would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Yates, Jr. et al to include the use of subroutines and loops.

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Yates, Jr. et al by the teachings of Spix et al and Chung et al, because the use of loops allows the breaking up of loops and the use of subroutines allow for easier context switch/state saving and thus avoiding delays in committing a context switch.

As per claim 7, Yates, Jr. et al discloses wherein said second native instruction comprises a pointer to a subroutine that performs functions associated with said first code sequence of native instructions and that provides the effective instruction pointer value for said non-native instruction (Column 75, lines 36-38).

As per claim 20, Chung et al discloses wherein said first code sequence of native instructions calls said second code sequence of native instructions as a subroutine (Column 9, lines 47-54).

As per claim 21, Chung et al discloses wherein said subroutine is callable by other code sequences other than said first code sequence (Column 8, lines 65- column 9, lines 2).

As per claim 22, Yates, Jr. et al discloses wherein said first address comprises a program counter value for said second native instruction and said second address comprises a program counter value for said first native instruction (Column 44, lines 23-29).

As per claim 26, Spix et al discloses wherein said translation comprises a first code sequence of native instructions that establishes conditions for a second code sequence of native instructions that execute in a loop (Column 44, lines 56-62).

As per claim 27, Yates, Jr. et al discloses wherein said address points to an instruction within said second code sequence, said instruction within said second code sequence having pointer bits that point to an instruction within said first code sequence, said instruction within said first code sequence having pointer bits that point to said effective instruction pointer (Column 44, lines 23-29).

As per claim 28, Chung et al discloses wherein said address points to an instruction within said second code sequence that has pointer bits that point to a subroutine that provides said effective instruction pointer (Column 9, lines 47-54).

Response to Arguments

6. Applicant's arguments filed 20 March 2006 have been fully considered but they are not persuasive.

Applicant argues "Yates does not anticipate the present claimed invention recited in independent Claims 1, 14 and 23. The context switch of Yates only switches from one X86 (e.g. non-native) thread to another X86 (e.g. non-native) thread. Hence the limitations of Claims 1, 14 and 23...which refer to both native and non-native instructions, are not 'part of the context switching described.' "

It is the contention of the examiner that Yates does indeed teach both types of context switches above, naming in sections C and D of part III of the description in the specification (See column 38, line 11- column 40, line 23). The context switch from one

type of thread to another is explicitly stated in column 38, lines 12-18 and column 39, lines 33-36. The two cited sentences describe the ability to switch from one to another. The cited lines in the office actions are directed to an example of a switch, which describes starting with a non-native thread, which then calls a native thread (and hence is a context switch), which then is interrupted and switched to a separate (and different) non-native thread. The original non-native thread and the native thread are then returned to upon completion. In this example, both types of context switches are exhibited. Given this interpretation, the applicant's argument is seen as non-persuasive.

Applicant also argues, "Yates does not show or suggest using a first address to locate a native instruction and using a second address to recover a non-native instruction, where these actions are performed in conjunction with a rollback operation." Applicant admits that Yates has "discussion [which] refers only to the EPC, which appears to be the native instruction pointer" and seems "to be no mention of a non-native instruction pointer."

Examiner would like to point to applicant column 38, lines 30-34, which describes a non-native instruction pointer (the AP register which is the argument pointer). Given this information, the applicant's argument is seen as non-persuasive.

Applicant further argues, "Yates does not show or suggest an indicator bit...in particular Yates does not show or suggest such a condition being applied to the recovery of a non-native instruction pointer."

In light of the above explanations on context switching and the existence of a non-native instruction pointer, it is evident that Yates does show a condition in which the recovery of a non-native instruction pointer may be done with a context switch and hence the argument is seen as non-persuasive.

Given the explanations above, it is the opinion of the examiner that the 103 rejections are indeed valid and thus is seen as non-persuasive.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

vl
May 23, 2006

Supervisory FRITZ FLEMING
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5/26/2006